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FEB 13 2004
PATENT & TRADEMARK OFFICE



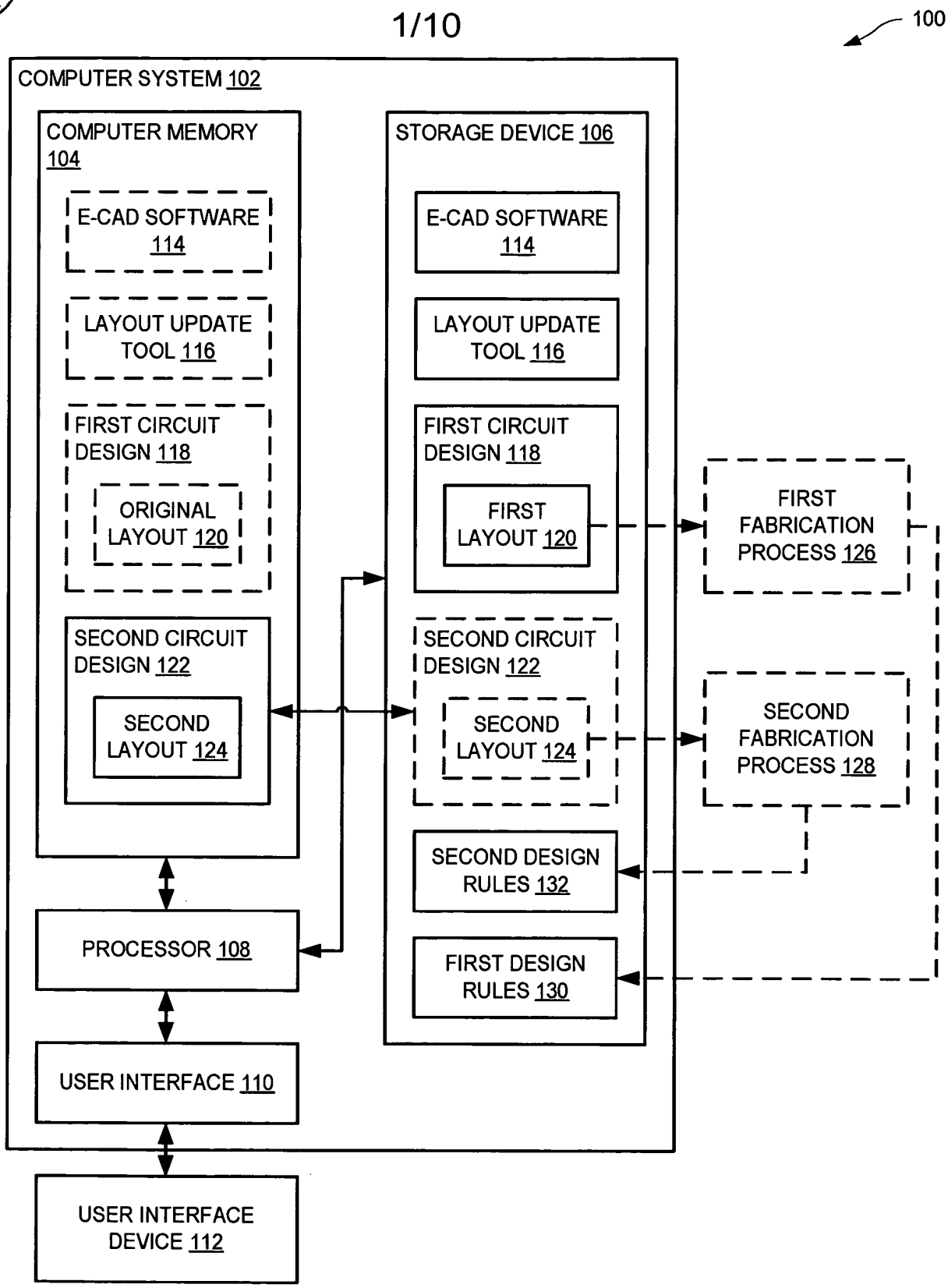



***FIGURE 1***

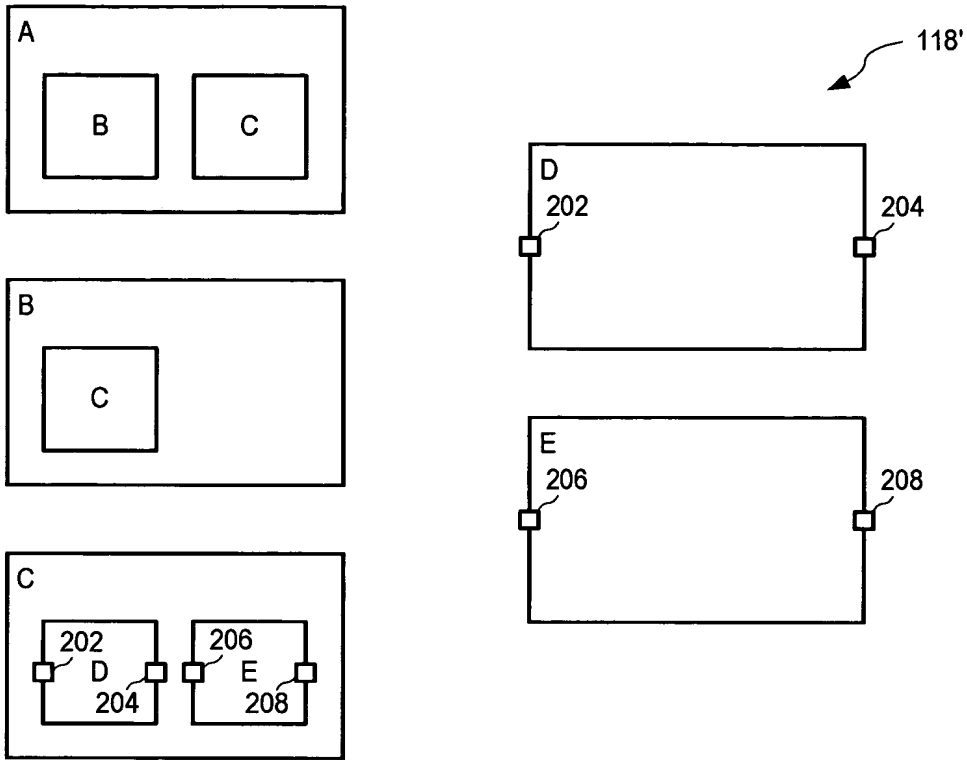



***FIGURE 2***

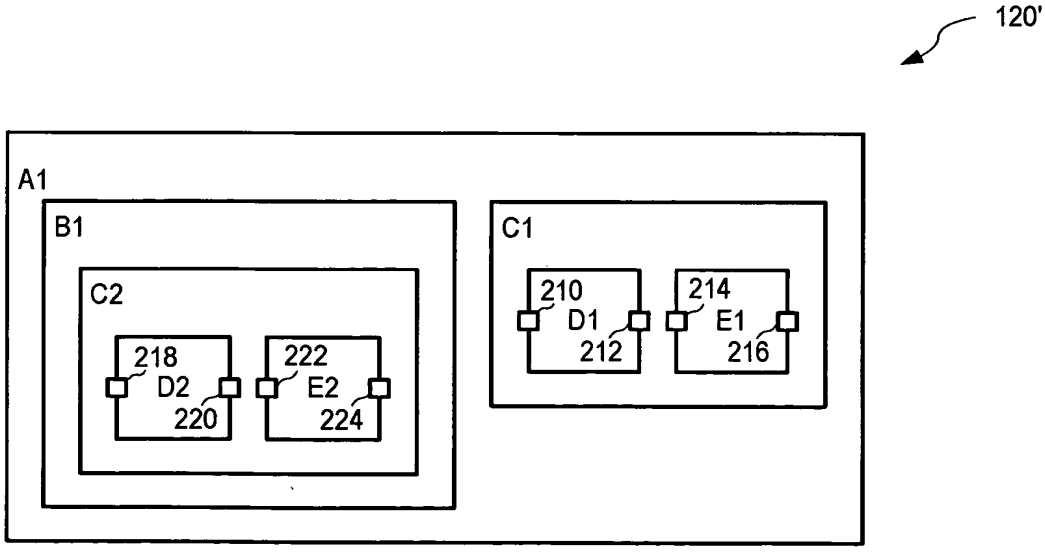



***FIGURE 3***

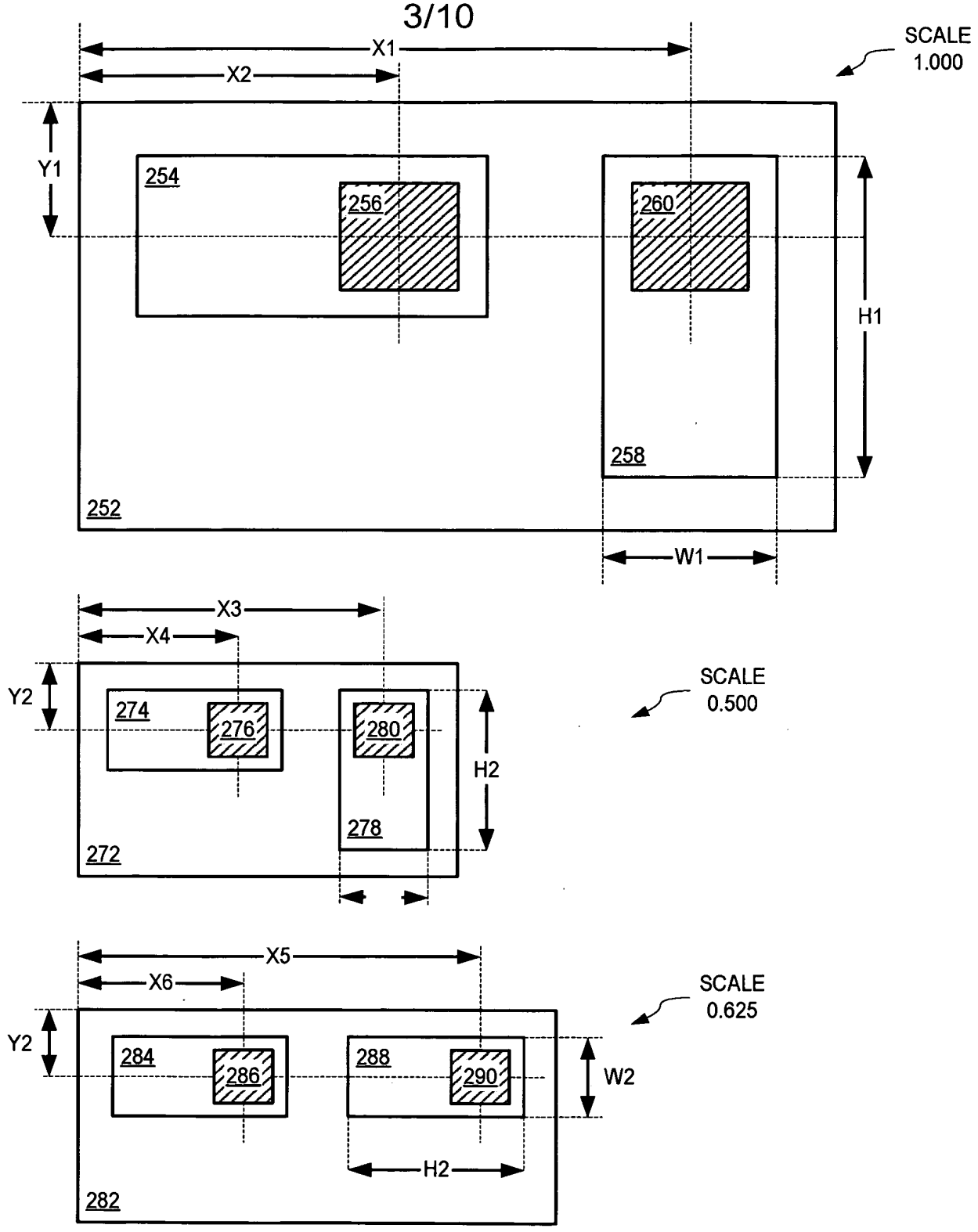

X1
X2
Y1
SCALE
1.000
254
256
260
H1
258
252
W1
X3
X4
Y2
SCALE
0.500
274
276
280
H2
278
272
X5
X6
Y2
SCALE
0.625
284
286
288
290
W2
H2
282

***Figure 4***

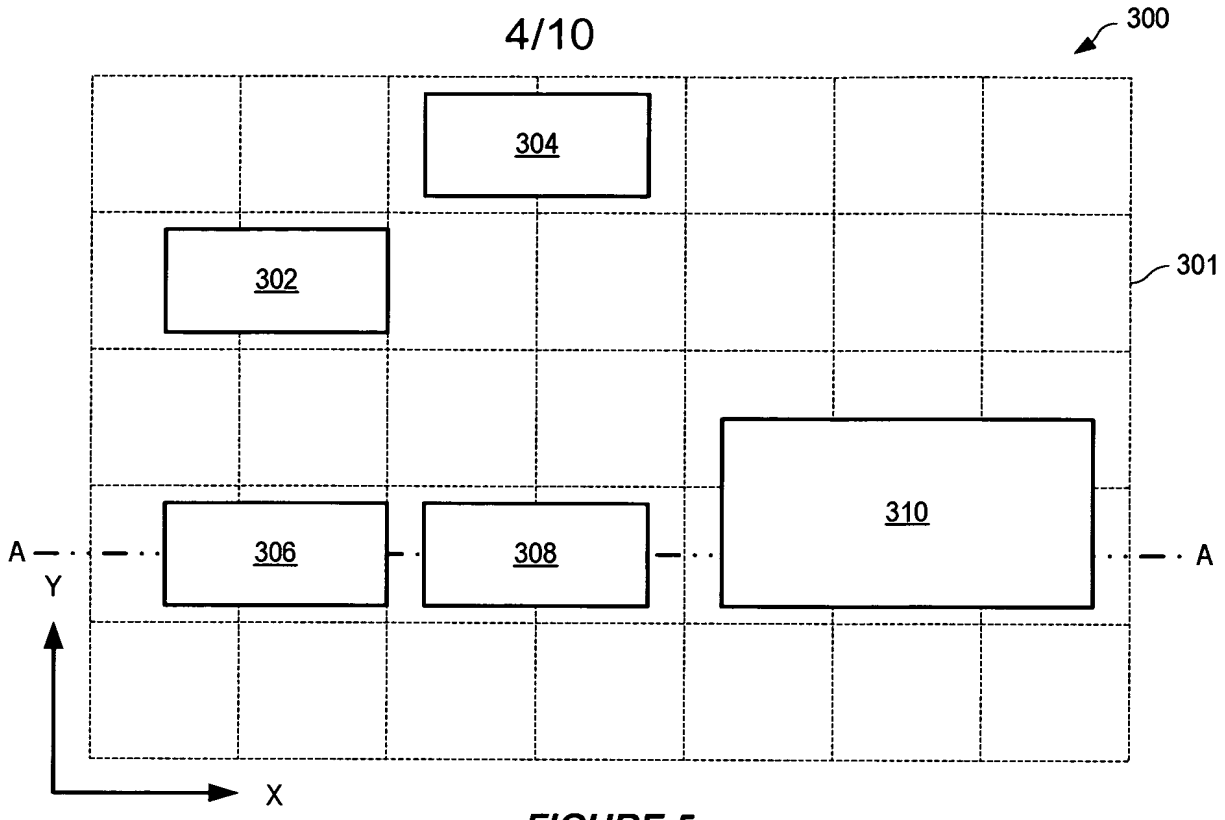



*FIGURE 5*

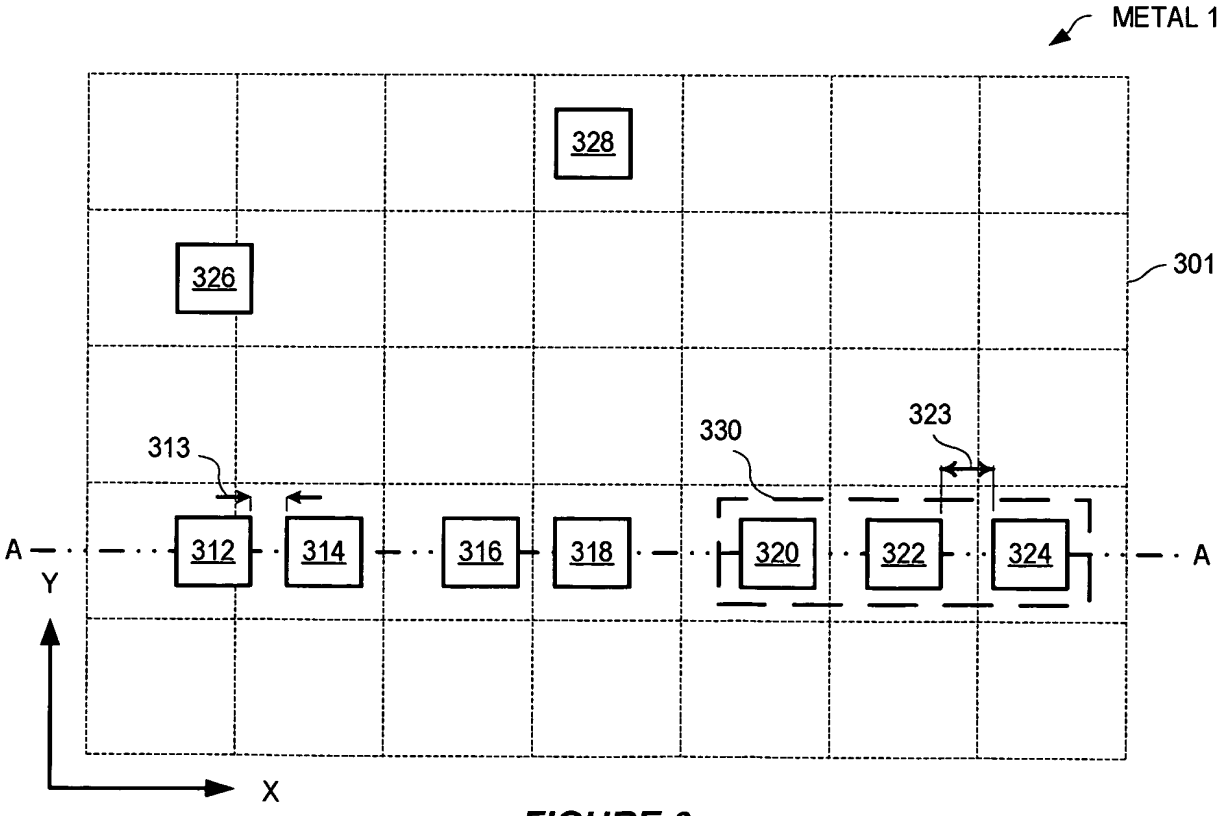



*FIGURE 6*

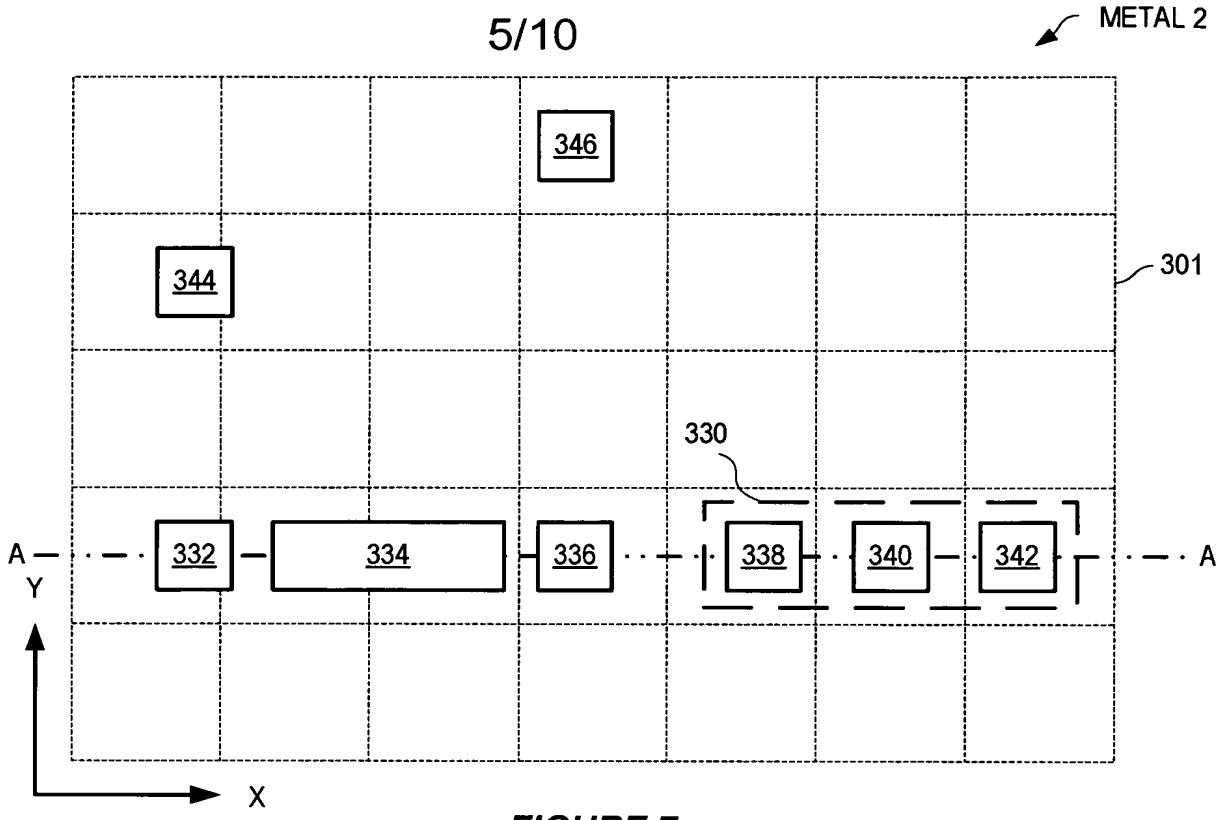



*FIGURE 7*

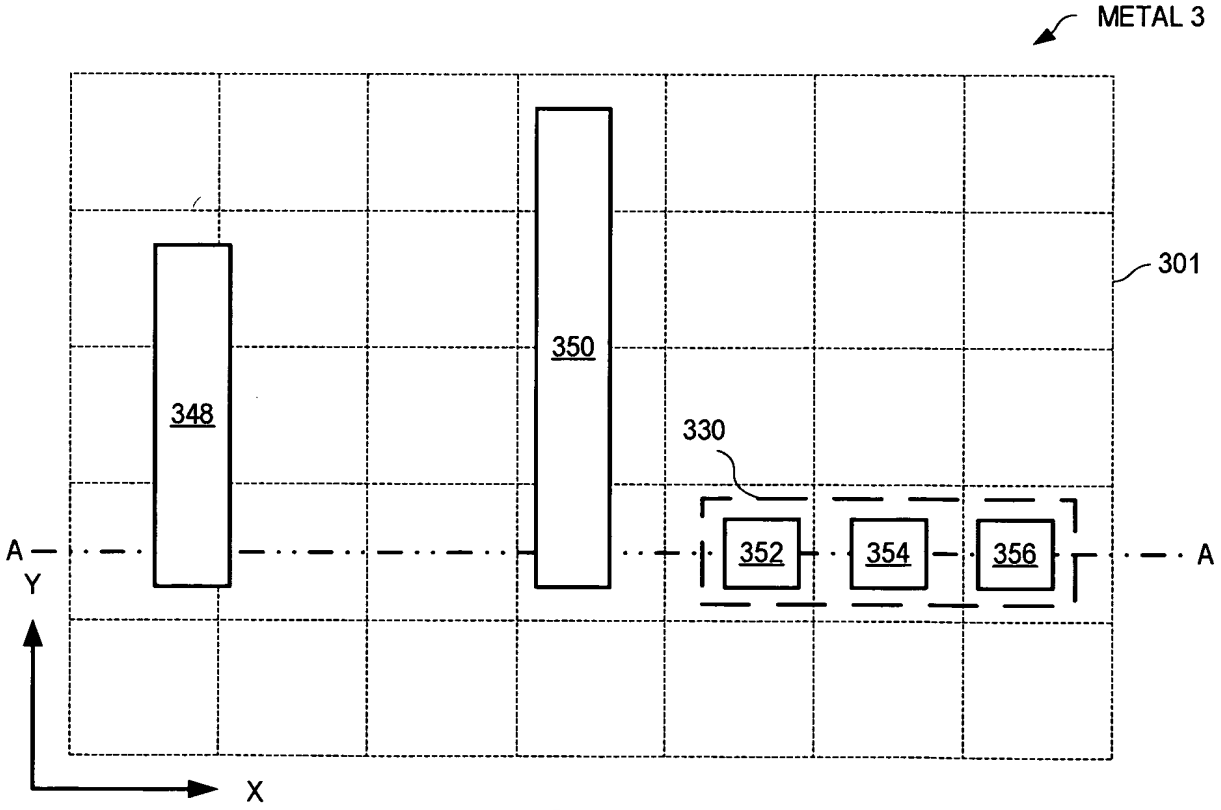



*FIGURE 8*

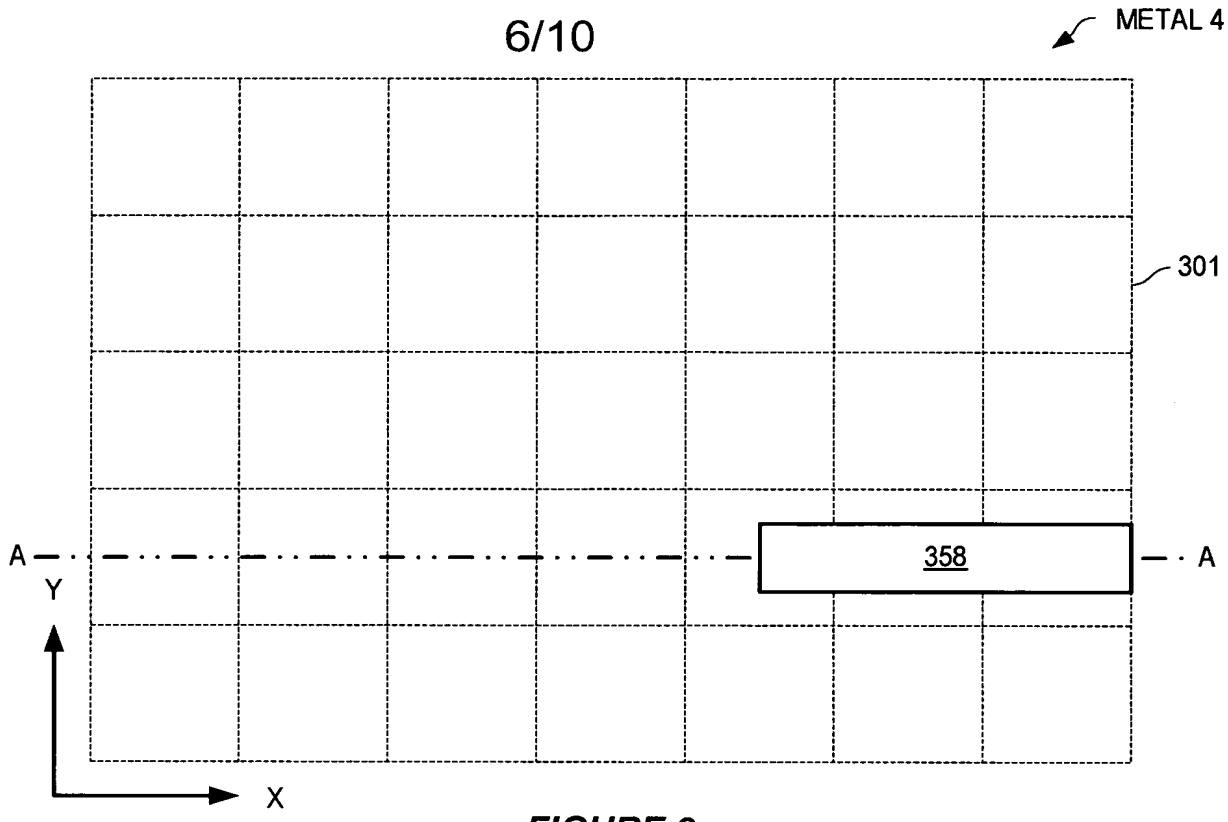



*FIGURE 9*

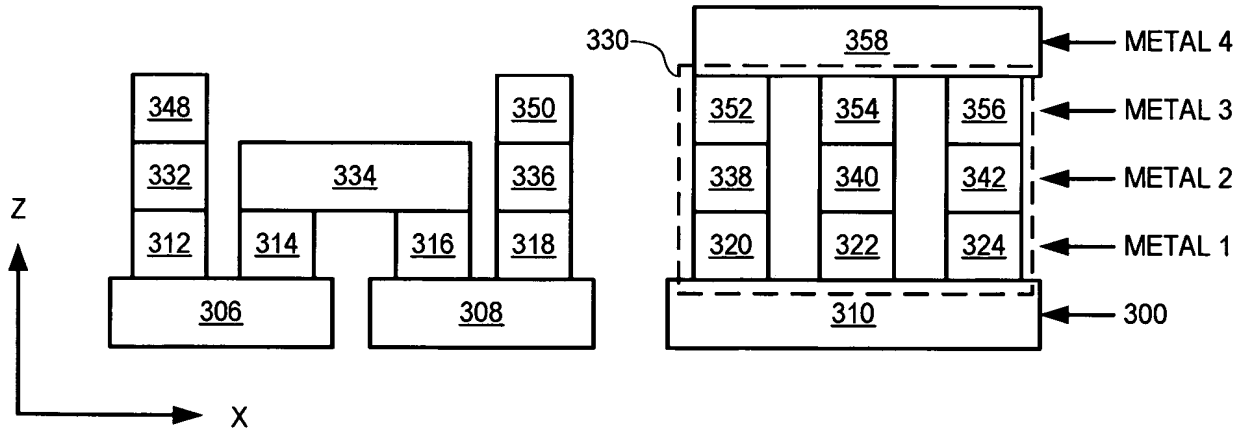



*FIGURE 10*

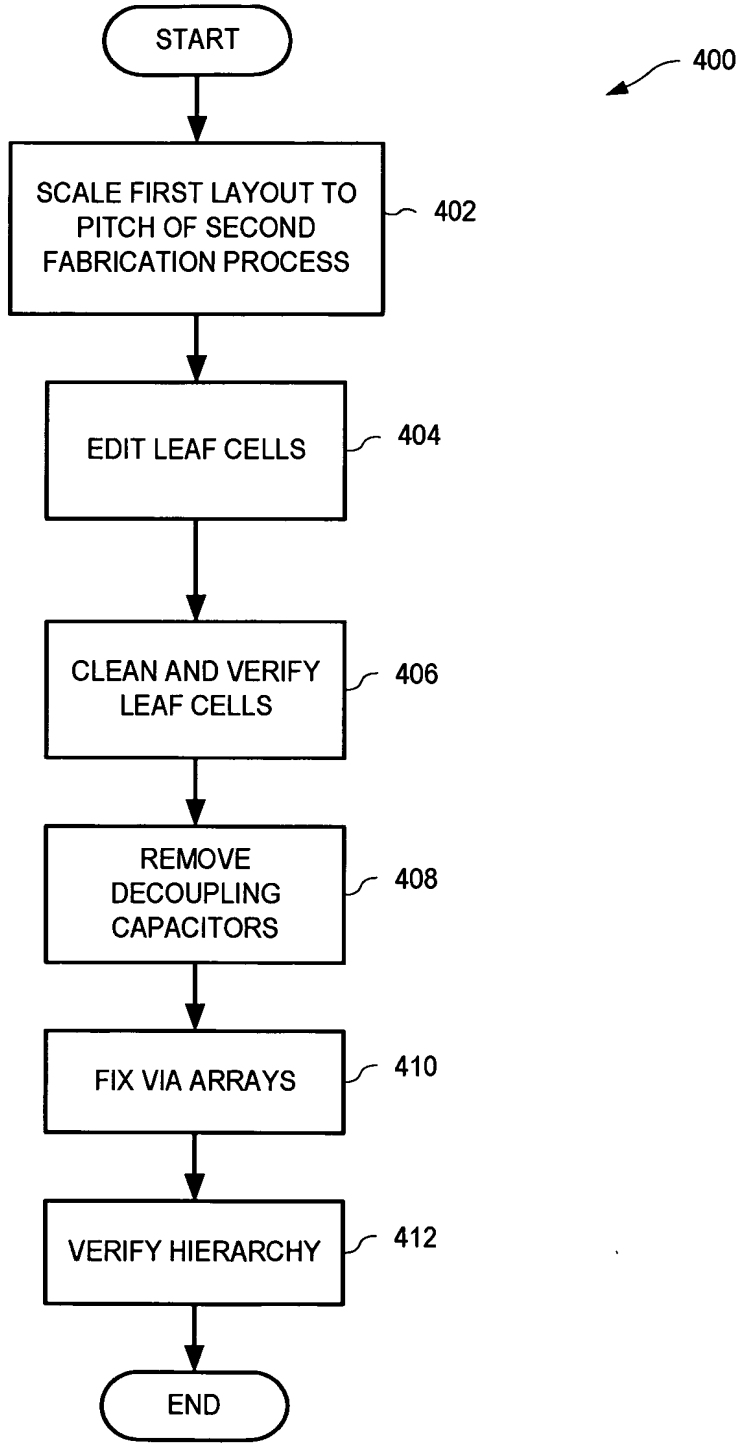

START
400
SCALE FIRST LAYOUT TO PITCH OF SECOND FABRICATION PROCESS
402
EDIT LEAF CELLS
404
CLEAN AND VERIFY LEAF CELLS
406
REMOVE DECOUPLING CAPACITORS
408
FIX VIA ARRAYS
410
VERIFY HIERARCHY
412
END

***FIGURE 11***

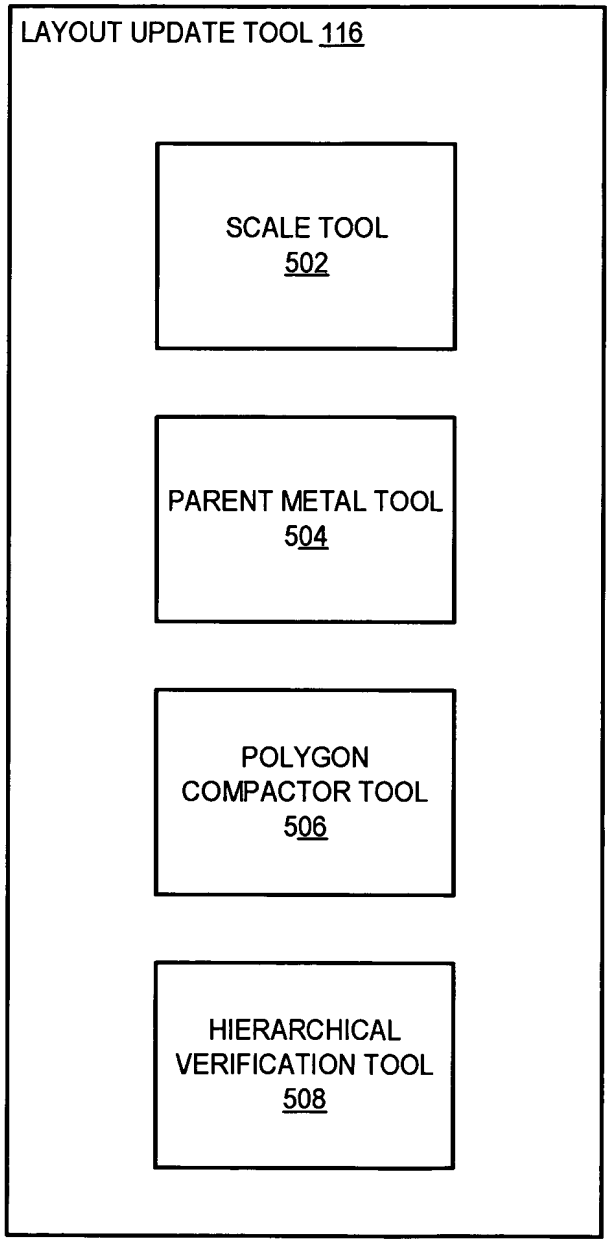
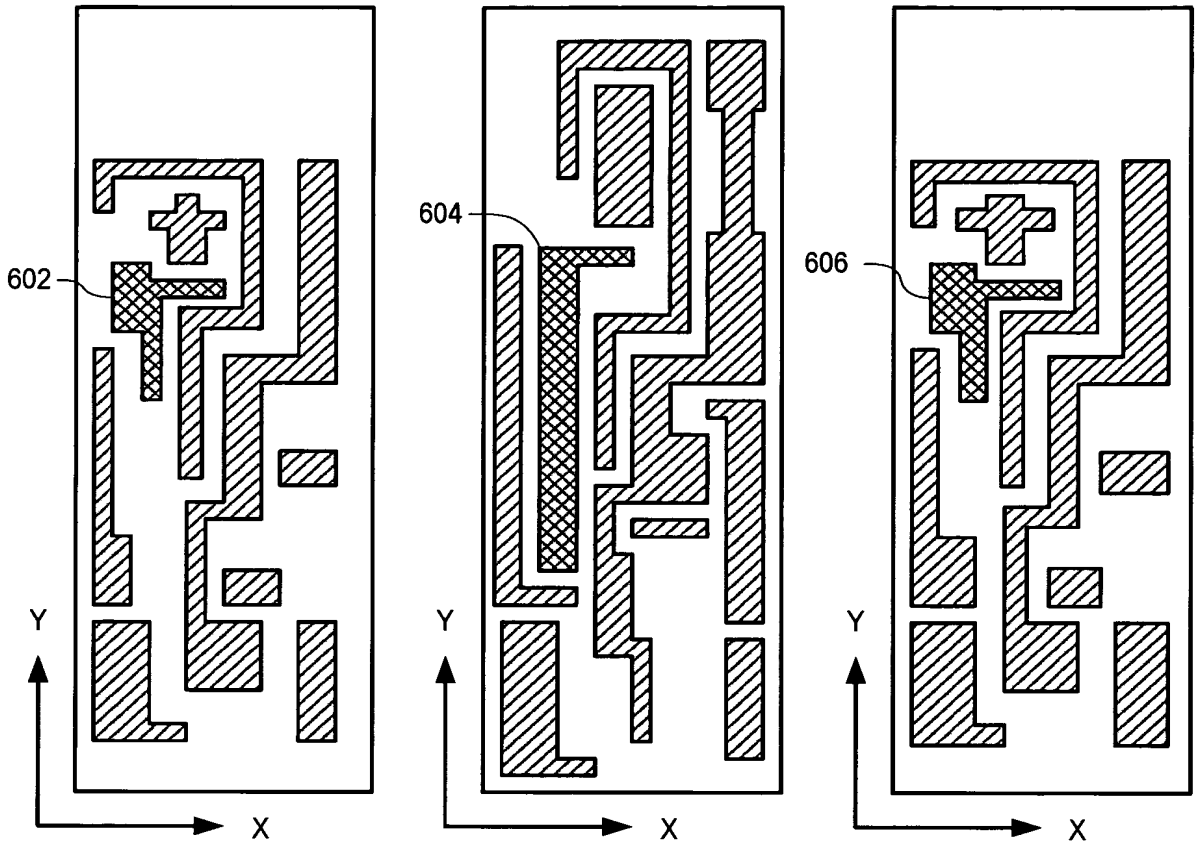

LAYOUT UPDATE TOOL 116
SCALE TOOL
502
PARENT METAL TOOL
504
POLYGON
COMPACTOR TOOL
506
HIERARCHICAL
VERIFICATION TOOL
508

***FIGURE 12***




CELL LAYOUT A

CELL LAYOUT B

CELL LAYOUT C

***FIGURE 13***

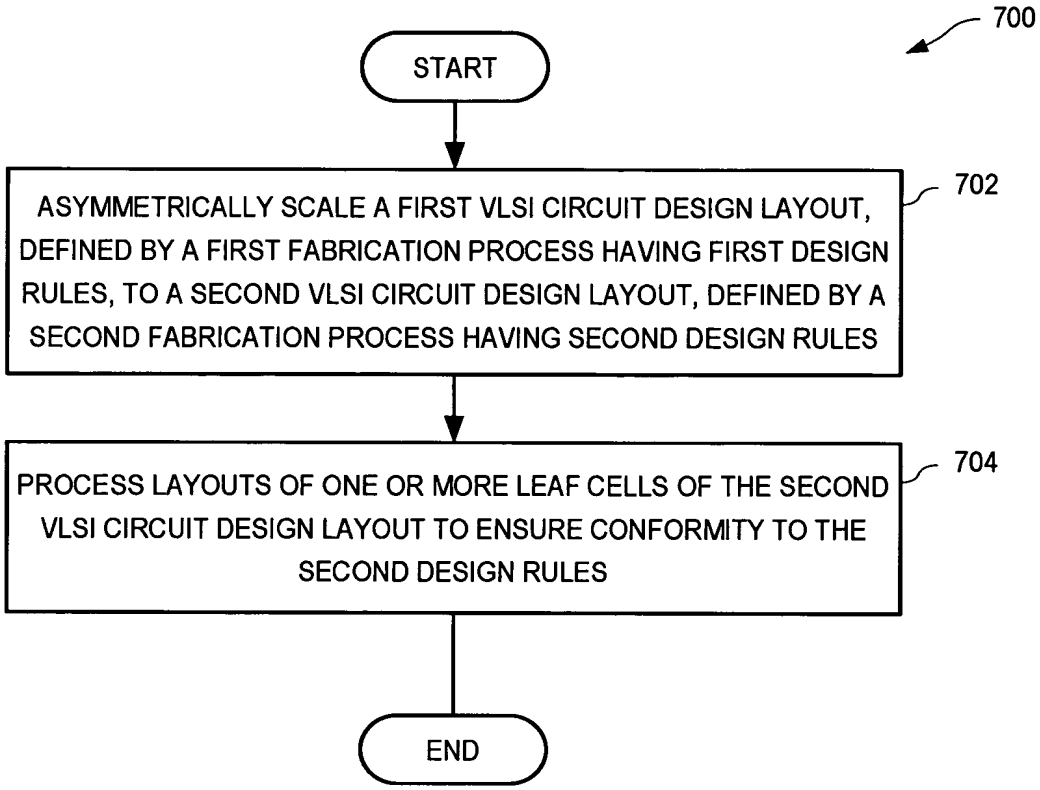

700
START
ASYMMETRICALLY SCALE A FIRST VLSI CIRCUIT DESIGN LAYOUT, DEFINED BY A FIRST FABRICATION PROCESS HAVING FIRST DESIGN RULES, TO A SECOND VLSI CIRCUIT DESIGN LAYOUT, DEFINED BY A SECOND FABRICATION PROCESS HAVING SECOND DESIGN RULES
702
PROCESS LAYOUTS OF ONE OR MORE LEAF CELLS OF THE SECOND VLSI CIRCUIT DESIGN LAYOUT TO ENSURE CONFORMITY TO THE SECOND DESIGN RULES
704
END

***Figure 14***